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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,381	12/12/2003	Jochen Beintner	YOR920030503US1	8534

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EXAMINER	
PERT, EVAN T	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,381	BEINTNER ET AL.	
	Examiner	Art Unit	
	Evan Pert	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28 and 37* is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-13,15,16,18,20-22,27 and 29* is/are rejected.

7)☒ Claim(s) *4,10,14,17,19,23-26 and 30-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1203*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to for deeming an ultra-thin silicon nitride layer as being "known to be electrically conductive" (e.g. claim 7; p. 4 at lines 15-18; p. 6, line 18 to p. 7, line 2; p. 7, lines 17-22; p. 8, lines 21-24).

In the specification, applicant may be ambiguously referring to an electrically conductive nitride, such as TaN, but the written description, as filed, does not support such a conclusion:

The only "nitride" named is "silicon nitride" with *written description* directed to an ultra-thin layer of "silicon nitride." Yet "silicon nitride" is a dielectric (insulator) that does not insulate well when it is very thin (Official Notice). A thin insulator is not "electrically conductive," so applicant is required to correct the misnomer of "silicon nitride" being "electrically conductive" just because it is "ultra-thin." In the art, an ultra-thin silicon nitride insulator as part of an electrically contiguous path is commonly referred to as a "tunneling contact," or the like, but not "electrically conductive." Correction is required.

2. The disclosure is objected to for a contradiction that is evidence of a lack of enablement for claim 27. In claim 27, "the silicon-containing layer sets the polysilicon grain size," as at lines 20-21 of p. 3. Yet, at p. 8, lines 14-17, the grain size "can be different," but "retains its grain size because of the ultra-thin nitride barrier." That is, the polysilicon grain size is determined by deposition conditions (e.g. temperature) that are independent of the silicon-containing layer, and so the disclosure does not adequately explain how the grain size of the polysilicon is "set by the silicon-containing layer."

Claim Rejections - 35 USC § 112

3. Claim 27 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to practice the invention. The specification particularly fails to direct one of skill to understand how "a silicon-containing layer *sets the grain size* of polysilicon," wherein a "nitride layer" is formed between the "polysilicon" and the "silicon-containing layer."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 3, 5, 6 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsukamoto et al. (US 4,931,897).

Regarding claim 1, the silicon-containing layer is 3, the nitride is 4 and the polysilicon is 6, wherein the "nitride" is clearly provided "between" 3 and 6.

In fact, for applicant's benefit, the examiner takes Official Notice that the semiconductor processing art is chock full of situations where a nitride layer is "between" a silicon-containing layer and polysilicon layer (Official Notice).

Regarding claim 2, the silicon-containing layer 3 is made "amorphous" (so it can be smoother), per col. 4, lines 50-59.

Regarding claim 3, the silicon-containing layer 3 is deposited as polysilicon and part is made amorphous so there is both an amorphous and polycrystalline layer that provide the silicon-containing layer.

Regarding claim 5, the polysilicon layer 3 made amorphous in its surface, necessarily has smaller grains than the polysilicon 6 (i.e. the layer 3 is amorphous at its surface to be smoother the polysilicon) [e.g. see Fig. 2].

Regarding claim 6, the silicon-containing layer 3 is formed below the polysilicon layer 6.

Regarding claim 29, see Fig. 2 showing first poly 3, second poly 6, with nitride 4 in between the 3 and 6 polysilicon layers.

6. Claims 1, 3, 6, 7, 8, 12, 20, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Anjum et al. (US 5,429,972).

Regarding claim 1, a semiconductor structure is formed (front cover) wherein a nitride layer is provided between a silicon-containing layer (bottom of polysilicon layer 22 that forms lower electrode of capacitor) and a polysilicon layer (i.e. upper layer of polysilicon 22), to form a capacitor as part of the semiconductor structure having a transistor.

Regarding claim 3, poly 22 is formed to provide the silicon-containing layer and the polysilicon layer.

Regarding claim 6, the silicon-containing layer is formed below the polysilicon layer.

Regarding claim 7, the nitride layer is a silicon nitride layer (col. 8, lines 25-27).

Regarding claim 8, the structure on the cover "includes a gate stack" because the gate to the left in the cover figure is a stack of oxide 16 under polysilicon 8, for example.

Regarding claim 12, polysilicon 22 is deposited as the silicon-containing layer.

Regarding claim 20, the poly 22 is deposited between 500°C and 600°C [col. 5, line 55], so the reference anticipates "below 550°C."

Regarding claim 21, the nitride layer is formed by anneal of poly 22 (implanted with nitrogen) per col. 8, lines 13-40.

Regarding claim 22, claim 6 of the reference indicates "exceeding 600°C," which anticipates "within the range of about 550°C to about 750°C."

7. Claims 1, 3, 6, 7, 8, 15 and 16 rejected under 35 U.S.C. 102(b) as being anticipated by Pourkeramati (US 5,953,254).

Regarding claims 1 and 3, the cover figure shows "nitride" formed between an (upper) "polysilicon" and a (lower) "polysilicon" silicon-containing layer in a gate stack semiconductor structure.

Regarding claim 6, the silicon-containing layer is "below" (see cover figure).

Regarding claim 7, the "nitride" in between the polysilicon layers is "silicon nitride" (col. 5, line 18).

Regarding claim 8, the structure includes a gate stack [e.g. col. 4, lines 41-44].

Regarding claim 15, the lower poly is deposited on a gate dielectric 210 and the gate dielectric 210 is formed on a substrate (e.g. "P-SUBSTRATE" of the cover figure).

Regarding claim 16, the substrate includes what is known as a "bulk" substrate 214 (i.e. a wafer) per col. 4, lines 46-47.

8. Claims 1, 3, 6, 7, 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Niroomand et al. (US 6,228,740).

Regarding claims 1 and 3, 16-20-18 in the cover figure is polysilicon-nitride-Polysilicon.

Regarding claim 6, 16 is below 18.

Regarding claim 7, the layer 20 is preferably "silicon nitride" per the paragraph bridging col. 10 to col. 11.

Regarding claim 9, nitride layer 20 is formed on a surface of silicon-containing layer 16 and a polysilicon layer 18 is formed on a surface of the nitride 20 [cover figure].

Regarding claim 12, the silicon-containing layer 16 is deposited as polysilicon, for example [col. 8, line 55].

Allowable Subject Matter

9. Claims 4, 10, 11, 14, 17, 19, 23-26, 28 and 30-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not disclose applicant's invention as disclosed in the specification characterized by the use of an ultra-thin silicon nitride layer between a silicon-containing layer and a polysilicon layer, wherein grain size of the polysilicon can be set without being affected by the silicon-containing layer.

Applicant's claimed invention, as a whole, can be distinguished from prior art, in the context of the *written description*, by various aspects not suggested in the prior art including: 1) the ultra-thin nitride 5 to 15 angstroms thick (e.g. claims 14 and 31), 2) small grain size of the silicon-containing layer within a range of about 10 nm to 20 nm (e.g. claims 10, 11, 28, 30 and 37), 3) the first and second polysilicon regions having differing grain sizes in a gate stack with ultra-thin nitride layer between the first and second regions (e.g. claims 32-35), and/or 4) process conditions and dimensions not suggested by the prior art, such conditions being desired only by hindsight from benefit of applicant's disclosure (e.g. claims 4, 17, 19, 23-25, 26 and 36).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
April 14, 2005

EVAN PERT
PRIMARY EXAMINER